REMARKS

By the present amendment, claim 1 has been amended to further clarify the concepts of the present invention. In addition, pending claims 2-4, 6-12, 14-18 and 20 have been cancelled and claims 21 through 53 have been added. Entry of these amendments is respectfully requested.

By a separate sheet attached hereto, the fee necessitated by the presentation of additional claims has been calculated and a check in that amount is enclosed.

In the Action, claims 1-4, 6, 11, 14-18 and 20 were rejected under 35 USC § 102(e) as being anticipated by the newly cited patent to Smejkal et al. In addition, the same claims were rejected under 35 USC § 103(a) as being unpatentable over the patent to Smejkal et al in view of the patent to Szwarc et al. In making the former rejection, it was asserted that the Smejkal et al patent teaches the entire structure as set forth in the noted claims in Figure 3. In the latter rejection, it was acknowledged that the untrimmed embodiment shown in Figure 3 of the Smejkal et al patent would not meet the recitations of the dependent claims regarding forming the trimmed resistor. The Szwarc et al patent was then asserted to teach minimizing trim cuts. Reconsideration of this rejection in view of the above claim amendments and the following comments is respectfully requested.

Before discussing the rejection in detail, a brief review of the presently claimed invention may be quite instructive. The newly presented claims include the following sets of claims:

(1) Claims 1 and 21-32 which correspond to Fig. 6 and a fourth embodiment of the present invention. Independent claim 1 has been amended to include the recitation:

> "...a fused solder layer having a thickness of 2-10 μm on each surface of the electrodes...."

(2) Claims 33-44 which correspond to Fig. 4 and a second embodiment of the present invention. Independent claim 33 is the combination of prior claims 1 and 7, the latter of which was indicated as being allowable by the examiner.

(3) Claims 45-53 which correspond to Fig. 5 and third embodiment of the present invention. Independent claim 45 includes the recitation:

> "...a fused solder layer having a thickness of 2-10 μm on each surface of the electrodes;
>
> two wire sites disposed at both ends of a surface of the resistor opposite to the surface having the electrodes..."

It is submitted that the Smejkal et al patent, whether taken alone or in combination with the patent to Szwarc et al, does not teach or suggest the invention as defined in the present claims.

More particularly, claim 1 now includes the recitation "a fused solder layer having a thickness of 2-10 μm on each surface of the electrodes." It is submitted that neither the Smejkal et al patent or Szwarc et al patent discloses a fused solder layer having a thickness of 2-10 μm. According to the Smejkal et al patent, particularly Figure 7A thereof, solder coating 66, 68 is formed on both surfaces surrounding the conductive strips (electrodes) 30, 32 and resistive strip (resistor body) 28.

In accordance with the concepts of the present invention, a fused solder layer 131, 132 is formed on one surface of the electrode 121, 122 (see Figure 4, for example). The fused solder layer is formed by diffusing the fused solder into the surface of the metal strip, thereby producing excellent current stability characteristics as set forth in the subject specification at page 7, lines 9-17. According to the electrodes having the fused solder layer, excellent current stability can be obtained.

The subject resistor provides additional advantages by its specific construction. Among others, the fused solder layer is very thin (2-10 μm), and is only formed on a surface of the electrode. As a consequence, a thinner resistor device can be obtained as

compared with the resistor device of the Smejkal et al patent which has solder coating 66, 68 on both sides. With a thinner resistor device, high density mounting can be realized by one side soldering when fixing the electrode onto circuit board. Further, manufacturing costs are reduced because the final process of solder coating is not required by initial process of fused soldering.

For the reasons stated above, withdrawal of the rejections under 35 U.S.C. § 103 and allowance of claims 1 and 21 through 53 over the cited patents are respectfully requested.

Applicants acknowledge with appreciation the indication that claims 7-10 and 12 were only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

In view of the foregoing, it is submitted that the subject application is now in condition for allowance and early notice to that effect is earnestly solicited.

Should the examiner deem that any further action by applicants would be desirable to place the application in better condition for allowance, the examiner is encouraged to telephone applicants' undersigned attorney.

In the event this paper is not timely filed, the undersigned hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 01-2340, along with any other additional fees which may be required with respect to this paper.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

Donald W. Hanson
Attorney for Applicants
Reg. No. 27,133

Atty. Docket No. 010481
Suite 1000, 1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

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Version with Markings to Show Changes Made

1. (Thrice Amended) A low resistance value resistor comprising:

a resistor body comprised by a resistive alloy;

at least two electrodes, comprised by metal strips of flat tetragonal shape having a high electrical conductivity, each of said metal strips having a same width with a width of said resistor body, and affixed on one surface of the resistor body separately wherein a diffusion layer is formed at an interface between the resistor body and the metal strip or in an interior of the resistor body under the metal strip;

a fused solder layer having a thickness of 2-10 μm on each surface of the electrodes; and

a straight and uniform current path formed in the resistor body between said at least two electrodes ~~having uniform electric potentials through the electrode, wherein said current path has a same width with the width of the resistor body and the electrodes~~.